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10/578,686	05/09/2006	Satoshi Yamanaka	1190-0625PUS1	3665
2292 7590 09/18/2009 BIRCH STEWART KOLASCH & BIRCH PO BOX 747 FALLS CHURCH, VA 22040-0747				
EXAMINER PATEL, JAYESH A				
ART UNIT		PAPER NUMBER		
2624				
NOTIFICATION DATE		DELIVERY MODE		
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

# Office Action Summary

**Application No.**

10/578,686

**Applicant(s)**

YAMANAKA ET AL.

**Examiner**

JAYESH PATEL

**Art Unit**

2624

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 09 May 2006.  
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☐ Claim(s) 1-11 and 13-20 is/are rejected.  
7) ☐ Claim(s) 12 is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
10) ☒ The drawing(s) filed on 09 May 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☒ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☒ Information Disclosure Statement(s) (PTO/5508)  
Paper No(s)/Mail Date 09/08, 08/06 and 05/06  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_  
5) ☐ Notice of Informal Patent Application  
6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Claim Objections***

Claim 1 is objected to because of the following informalities: At lines 4-5 "a mean value" should read "the mean value" and "a plurality of pixels" should read "the plurality of pixels". Appropriate correction is required.

### ***Double Patenting***

Claim 11 is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 9. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim 10 is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 12. Claim 12 includes all the limitations from claim 10 therefore it should be canceled. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 7-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 7 recites the limitation "k-i" in line 5. It is unclear as to what is the value of "k-i" as i is not defined in claims 2 or 7. Claims 8-12 depends directly or indirectly on claim 7 therefore they are rejected. Also the recital of the limitations of Claim 2 and Claim 1 should be incorporated in to claim 7 if it is to be treated as an independent claim as the introductory sentence in the preamble is different from claims 1 and 2. for the purpose of examination the examiner has interpreted claim 7 dependent on claims 2 and 1.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Chen (US 6570616) hereafter Chen.

1. Regarding claim 1, Chen discloses a mean preserving interpolation calculation circuit (**Fig 1**) that obtains interpolation data for a missing pixel such that a mean value of a plurality of pixels constituting a group of pixels including the missing

pixel (**Fig 6 consists of two dimensional pixel array which includes the group of pixels which includes the missing pixel G33 and the neighboring pixels G23,G32,G43 and G34**) is equal to a mean value of a plurality of pixels constituting a group of pixels not including the missing pixel (**the value of the missing pixel G33 is equal to the average or mean value of the neighboring pixels (G23+G43+G32+G34)/4 and does not include the missing pixel G33 in the calculation at Col 8 Line 55 and equation 8 at Col 10**).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 2-6 and 13-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Lin et al. (US 20040208384) hereafter Lin.

2. Regarding claim 2, Chen discloses the mean preserving interpolation calculation circuit of claim 1. Chen discloses wherein the number of pixels constituting the group of pixels including the missing pixel and the number of pixels constituting the group of pixels not including the missing pixel are both (**Fig 6 which consists of 5X5 array of pixels including the missing pixel in the two dimensional array**), however is silent and does not recite in exact claim

language the mean preserving interpolation calculation circuit comprising: an incomplete total calculation circuit for obtaining a total of values of the pixels other than the missing pixel in the k pixels constituting the group of pixels including the missing pixel; a complete total calculation circuit for obtaining a total of values of the k pixels constituting the group of pixels not including the missing pixel; and a difference circuit for obtaining interpolation data for the missing pixel by subtracting an output of the complete total calculation circuit from an output of the incomplete total calculation circuit.

Lin discloses the mean preserving interpolation calculation circuit comprising: an incomplete total calculation circuit for obtaining a total of values of the pixels other than the missing pixel (**summation of the pixels in the field  $F(n-1)$  at para 0037**) in the k pixels constituting the group of pixels including the missing pixel (**Lin discloses the SAD which is the total of the pixels in the neighborhood at para 0037-0039 where the four fields are part of the frame (MXN) which include the missing pixel**); a complete total calculation circuit for obtaining a total of values of the k pixels constituting the group of pixels (**summation of the pixels in the field  $F(n+1)$  at para 0037**) not including the missing pixel (**field  $F(n+1)$  does not include the missing pixel in the total as the missing pixel is in the field  $F(n)$** ); and a difference (**difference between the fields as seen in Para 0037-0039**) circuit for obtaining interpolation data for the missing pixel by subtracting an output of the complete total calculation circuit from an output of the incomplete total calculation circuit. Lin discloses the

interpolation of the missing pixel by correctly evaluating the missing pixel in the static or non-static region such that the reconstruction errors are minimized (hardly recognizable) at **paras 0015-0016**. Lin and Chen are from the same field of endeavor and are analogous art therefore it would be obvious for one of ordinary skill in the art at the time the invention was made to have used the teachings of Lin in the missing pixel value calculation circuit of Chen for the above reasons.

3. Regarding claim 3, Chen and Lin disclose the mean preserving interpolation calculation circuit of claim 2. Lin discloses the summation of the pixels in the fields in **para 0037-0039** and the **summation and averaging in para 0005** meeting the limitations of claim 3.

4. Regarding claim 4, Chen and Lin disclose the mean preserving interpolation calculation circuit of claim 2. Lin discloses static and non-static region (**paras 0015,0016 and para 0004**) which meets the limitation of wherein each said group of pixels constitutes a portion of a periodically varying series of pixels.

5. Regarding claim 5 see the explanation of claim 4.

6. Regarding claim 6, Chen and Lin disclose the pixel interpolation circuit comprising the mean preserving interpolation calculation circuit of claim 1. Lin

disclose further comprising a circuit using maximum and minimum values of pixels in a neighborhood of the missing pixel to limit the output range (**in para 0044 where the calculation of pixel differences larger and smaller than the threshold meets the limitation of maximum and minimum values of pixels**).

7. Claim 13 is a corresponding method claim of claim 1. See the explanation of claim 1.

8. Claim 14 is a corresponding method claim of claim 2. See the explanation of claim 2.

9. Claim 15 is a corresponding method claim of claim 3. See the explanation of claim 3.

10. Claim 16 is a corresponding method claim of claim 4. See the explanation of claim 4.

11. Claim 17 is a corresponding method claim of claim 5. See the explanation of claim 5.

12. Claim 18 is a corresponding method claim of claim 6. See the explanation of claim 6.



Claims 7-9, 11 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Lin and in further view of Sasaki et al (US 7206021) hereafter Sasaki as best understood by the examiner.

**13.** Regarding claim 7, Chen and Lin disclose a pixel interpolation circuit comprising a plurality of mean preserving interpolation calculation circuits as recited in claim 2. Chen and Lin together disclose wherein the mean preserving interpolation calculation circuits have different values of said k as seen in claim 2, however are silent and do not recite in exact claim language further comprising an output circuit, the plurality of mean preserving interpolation calculation circuits generating respective interpolation data for the missing pixel, the output circuit selecting one of the interpolation data output by the plurality of mean preserving interpolation calculation circuits and outputting the selected data as the interpolation data for the missing pixel.

Sasaki discloses an output value Dc (Fig 1-2) produced as a result of multiple pixel interpolating circuits 4 sub 1 to 4 sub n and each interpolating circuits 4 sub 1 through 4 sub n producing the average values of the neighboring pixels (**Fig 3 where the value of pixel Pc is the average value of 3X3 pixels (region 31) or 5X5 pixels (region 32) having different values of k (pixels)) at (Col 7 lines 63 through Col 8 lines 20).** Sasaki further disclose the output as a result of multiple interpolating circuits in section (5 and 7 Fig 1). Sasaki discloses

that the optimum pixel interpolating process can be executed by the respective compensation of their disadvantages and emphasizing their advantages over one another by the multiple interpolation circuits 4 sub 1 through 4 sub n and as such the output of high quality can be obtained at **Col 7 lines 13-27**. Sasaki, Chen and Lin are from the same field of endeavor (interpolating pixels) and are analogous art (image processing), therefore it would be obvious for one of ordinary skill in the art at the time the invention was made to have used the teachings of Sasaki in the mean preserving circuit of Chen and Lin for the above reasons.

**14.** Regarding claim 8, Chen, Lin and Sasaki disclose the pixel interpolation circuit of claim 7. Sasaki disclose further comprising an adjacent pixel mean interpolation calculation circuit for generating the mean value of pixels adjacent to the missing pixel as interpolation data (**Fig 2 which discloses the interpolating circuit 4 sub 1 having an averaging or mean calculation part 10 and Fig 3 which discloses the missing or current pixel and adjacent pixels which are used for calculating mean or average**), wherein the output circuit selects one of the interpolation data output by the plurality of mean preserving interpolation calculation circuits and the adjacent pixel mean interpolation calculation circuit and outputs the selected data as the interpolation data for the missing pixel (**Fig 1 and Col 7 lines 28-40 where output interpolated data Dc is disclosed**).

15. Regarding claim 9, Chen, Lin and Sasaki disclose the pixel interpolation circuit of claim 8. Sasaki disclose further comprising a selection signal generator generating a selection signal for selecting one of the data from the plurality of interpolation calculation circuits based on original data of a pixel in a neighborhood of the missing pixel and interpolation data obtained for the pixel in the neighborhood of the missing pixel by methods identical to the methods by which the interpolation data for the missing pixel are obtained (**interpolating circuits 4 sub 1 through 4 sub n (Fig 1) are all identical and perform identical methods of generating mean or average interpolated signal AV1-AVn by different sampling of the pixel arra as seen in Fig 2**).

16. Regarding claim 11 see the explanation of claim 9.

17. Claim 19 is a corresponding method claim of claim 7. See the explanation of claim 7.

18. Claim 20 is a corresponding method claim of claim 8. See the explanation of claim 8.

***Allowable Subject Matter***

Claim 12 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Other Cited Prior art***

The other cited prior art pertinent to applicant's disclosure but not relied on are (US 6278803), (US 6882365), (US 7102673), (US 5832143), (US 20050010621), (US 7136541), (US 6744916), (US 5481311), (US 6738498), (US 6768512), (US 20020167602), (US 6091862) and (US 20060050990).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAYESH PATEL whose telephone number is (571)270-1227. The examiner can normally be reached on 5-4-9.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Werner can be reached on 571-272-7401. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public

PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

08/31/2009  
/JAYESH PATEL/  
Examiner, Art Unit 2624

/Brian P. Werner/  
Supervisory Patent Examiner, Art Unit 2624